X3 Datasheet

Quad-Core Application Processor

Version 1.0

Nov.2,2019

Revision History

Version	Date	Description
V1.0	2019-11-08	Initial release version

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1. Overview

The ARTMEMTECH X3 is a quad-core HMI application processor that based on ARM Cortex™-A7 CPU together with Mali400MP2 GPU architecture.

Main features of X3 include:

CPU architecture:X3 is based on quad-core Cortex™-A7 CPU architecture to deliver superior system performance as well as optimized battery life experience,in that Cortex™-A7 is the most power efficient CPU core ARM's ever developed;

Graphic:X3 adopts the extensively implemented and technically mature Mali400MP2 GPU to provide end users with optimal experience in web browsing,video playback and games; OpenGL ES 2.0 and OpenVG 1.1 standards are supported;

Video Engine:X3 supports high-definition 1080P video processing, and supports various mainstream video standards such as H.264,VP8,MPEG 1/2/4,JPEG/MJPEG,etc;

Display:X3 supports CPU/RGB/LVDS LCD interface up to 1280x800 resolution.Four-lane MIPI DSI(Display Serial Interface)is integrated as well, supporting MIPI DSI V1.01 and MIPI D-PHY V1.00;

Image:X3 supports a parallel CMOS sensor interface up to 5M resolution.

Thanks to its advanced system design and outstanding software optimization,the X3 is capable of providing top-notch system performance with long-lasting battery life experience:in addition to its energy-efficient Cortex™-A7 CPU architecture,advanced fabrication process,video acceleration hardware,DVFS technology support and high system integration.Additionally,X3 features high system integration with a wide range of integrated I/Os like 4-lane MIPI DSI,LVDS,USBOTG,USB HOST,SD/MMC,I2S/PCM,thus significantly reducing system components required in design to simplify product design and reduce total system costs.

2. Feature

2.1. CPU Architecture

The quad-core X3 platform is based on ARM's Cortex™-A7 CPU architecture.

- ARMv7 ISA standard instruction set plus Thumb-2 and Jazeller RCT
- NEON with SIMD and VFPv4 support
- Support hardware virtualization
- Support LPAE
- Integrated 32KB L1 instruction cache and 32KB L1 data cache for each CPU
- Shared 512KB L2 cache
- Support DVFS with independent power domain

2.2. GPU Architecture

- ARM Mali400MP2 GPU
- Support OpenGL ES 2.0/OpenVG 1.1 standard

2.3. Memory Subsystem

Boot ROM

- Support system boot from Raw NAND,eMMC,SPI Nor Flash,SD/TF card
- Support system code download through USB OTG

SDRAM

- SIP 128MB 16bit DDR3,1 rank
- Clock frequency up to 672MHz
- Support Memory Dynamic Frequency Scale

NAND Flash

- Comply to ONFI 2.3 and Toggle 1.0
- Up to 64-bit ECC per 512 bytes or 1024 bytes
- 8-bit Raw NAND flash controller sharing pin with eMMC
- Up to 2 CE and 2 RB signals
- Support SLC/MLC/TLC NAND and EF-NAND
- Support SDR/ONFI DDR/Toggle DDR NAND

SD/MMC Interface

- Up to three SD/MMC controllers
- Comply to eMMC standard specification V4.41,SD physical layer specification V2.0,SDIO card specification V2.0
- 1-bit or 4-bit data bus transfer mode for SD and SDIO cards up to 50MHz
- 1-bit,4-bit or 8-bit data bus transfer mode for MMC cards up to 50MHz in SDR modes

2.4. System Peripherals

Timer

- Support two timers:clock source can be switched over 24MHz and 32768Hz
- Support two 33-bit AVS counters
- Support one 64-bit system counter from 24MHz
- Support watchdog to generate reset signal or interrupts
- High Speed Timer
- Clock source is fixed to AHB1,and the pre-scale ranges from 1 to 16
- Support one 56-bit counter

RTC

- Timer,Calendar,Alarm
- Support full clock features:second/minute/hour/day/month/year(with leap year)
- Support 32768Hz clock fanout

GIC

- Support 16 SGIs,16 PPIs and 128 SPIs
- Support ARM architecture security extensions
- Support ARM architecture virtualization extensions
- Support single processor and multiprocessor environments

DMA

- 8-channel DMA
- Support data width of 8/16/32 bits
- Support linear and IO address modes
- Support data transfer types with memory-to-memory,memory-to-peripheral,peripheral-to-memory

CCU

- 11 PLLs
- 24MHz oscillator,a 32768Hz oscillator and an on-chip RC oscillator
- Support clock gating control for individual components
- Clock generation,clock division,clock output

PWM

- Up to 2 PWM outputs
- Support cycle mode and pulse mode
- The pre-scale is from 1 to 16
- Security System
- Support Symmetrical Algorithm:AES,DES,TDES(3DES)
- Support Hash Algorithm:SHA-1,MD5
- Support 160-bits hardware PRNG with 175-bits seed
- Support ECB,CBC,CTR modes for DES/3DES

- Support ECB,CBC,CTR,CTS modes for AES
- Support 128-bits,192-bits and 256-bits key size for AES
- 32-words RX FIFO and 32-words TX FIFO for high speed application
- Support CPU mode and DMA mode

2.5. Display Subsystem

Display Engine

- Four movable layers,each layer size up to 2048x2048 pixels
- Ultra-Scaling engine

  --4-tap scale filter in horizontal and vertical

  --Support input size up to 2048x2048 resolution and output size up to 1280x1280 resolution
- Support multiple image input formats:1/2/4/8-bpp mono/palette,16/24/32-bpp color,YUV444/420/422/411
- Support alpha blending/color key/gamma
- Support output color correction:luminance/hue/saturation,etc
- Support Saturation Enhancement and Dynamic Range Control
- Support real time write back function

Video Output

- Support RGB/CPU/LVDS LCD interface up to 1280x800 resolution
- Integrated 4-lane MIPI DSI interface up to 1280x800 resolution

  --Support MIPI DSI V1.01 and D-PHY V1.00

  --Support command mode and video mode(non-burst mode with sync pulses,non-burst mode with sync event and burst mode)

--Support pixel format:RGB888,RGB666,loosely RGB666 and RGB565

Dither function from RGB666/RGB565 to RGB888

2.6. Video Engine

Video Decoding

- Support video playback up to 1920x1080@60ps
- Support multi-format video playback,including MPEG1/2,MPEG4 SP/ASP GMC,WMV9/VC1,H.263
- including Sorenson Spark,H.264 BP/MP/HP,VP8,JPEG/MJPEG,etc

Video Encoding

- Support H.264 HP video encoding up to 1920x1080@60fps
- JPEG baseline:picture size up to 4080x4080
- Support Alpha blending
- Support thumb generation
- 4x2 scaling ratio:from 1/16 to 64 arbitrary non-integer ratio

2.7. Video Input

CSI

- Support parallel camera sensor
- Support 8bit CCIR656 protocol
- Maximum still capture resolution to 5M
- Maximum video capture resolution to 1080p@30fps

2.8. Audio Subsystem

Analog Audio Codec

- Support stereo audio DAC
  --Up to 100dB SNR
  --8KHz to 192KHz DAC sample rate
- Stereo audio ADC
  --Up to 96dB SNR
  --8KHz~48KHz ADC sample rate
- Support three analog audio inputs
  --Two microphone differential inputs for main mic and headphone mic
  --One stereo line-in input for FM
- Support one analog audio outputs
  --One stereo or differential capless headphone output
- Support Dynamic Range Controller adjusting the DAC playback output(DRC)
- Support Automatic Gain Control adjusting the ADC recording output(AGC)
- Two PCM interface connected with BB and BT

Digital Audio

- Support two I2S/PCM compliant digital audio interfaces for modem and BT
- I2S or PCM configured by software
- Support 3 I2S Data formats:Standard I2S,Left Justified and Right Justified
- I2S supports 2 channels output and 2 channels input
- PCM supports 8/16-bit word length,8-bit u-law and A-law compress sample
- Sample rate from 8KHz to 192KHz
- Support 16,20,24bits audio data resolutions
- One 128x24-bits FIFO for data transmit,one 64x24-bits FIFO for data receive

2.9. External Peripherals

USB 2.0 OTG

- Support High-Speed(HS,480-Mbps),Full-Speed(FS,12-Mbps),and Low-Speed(LS,1.5-Mbps)in Host mode
- Support High-Speed(HS,480-Mbps)and Full-Speed(FS,12-Mbps)in Device mode
- Support up to 10 user-configurable endpoints for Bulk,Isochronous,Control and Interrupt
- Support the embedded DMA

USB Host

- EHCI/OHCI-compliant hosts
- USB2.0 PHY and HSIC
- Support High-Speed(HS,480Mbps),Full-Speed(FS,12Mbps),and Low-Speed(LS,1.5Mbps)Device
- An internal DMA Controller for data transfer with memory

KEYADC

- 6-bit resolution
- Support single key,normal key and continuous key

UART

- Five UART controllers
- FIFO size up to 64 bytes
- Support speed up to 3MHz
- Compliant with industry-standard 16550 UARTs
- Support Infrared Data Association(IrDA)1.0 SIR

SPI

- One SPI controller
- Master/Slave configurable
- Full-duplex synchronous serial interface
- Two 64-Bytes FIFO for SPI-TX and SPI-RX operation
- DMA-based or interrupt-based operation
- Polarity and phase of the chip select(SPI_SS)and SPI_Clock(SPI_SCLK)are configurable

TWI

- Up to four TWIs(Two Wire Interface)controllers
- One dedicated TWI for CSI
- Support Standard mode(up to 100K bps)and Fast mode(up to 400K bps)
- Master/Slave configurable
- Allows 10-bits addressing transactions
- RSBTM(Reduced Serial Bus)
- Speed up to 20MHz with lower power consumption
- Support Push-Pull bus
- Support Host mode
- Support multiple devices
- Programmable output delay of CD signal
- Parity check for address and data transmission

2.10. Package

- FBGA 262 balls,0.60mm ball pitch,16 x 13 x 1.0-mm

3. Block Diagram

The following figure shows the block diagram of X3 processor.

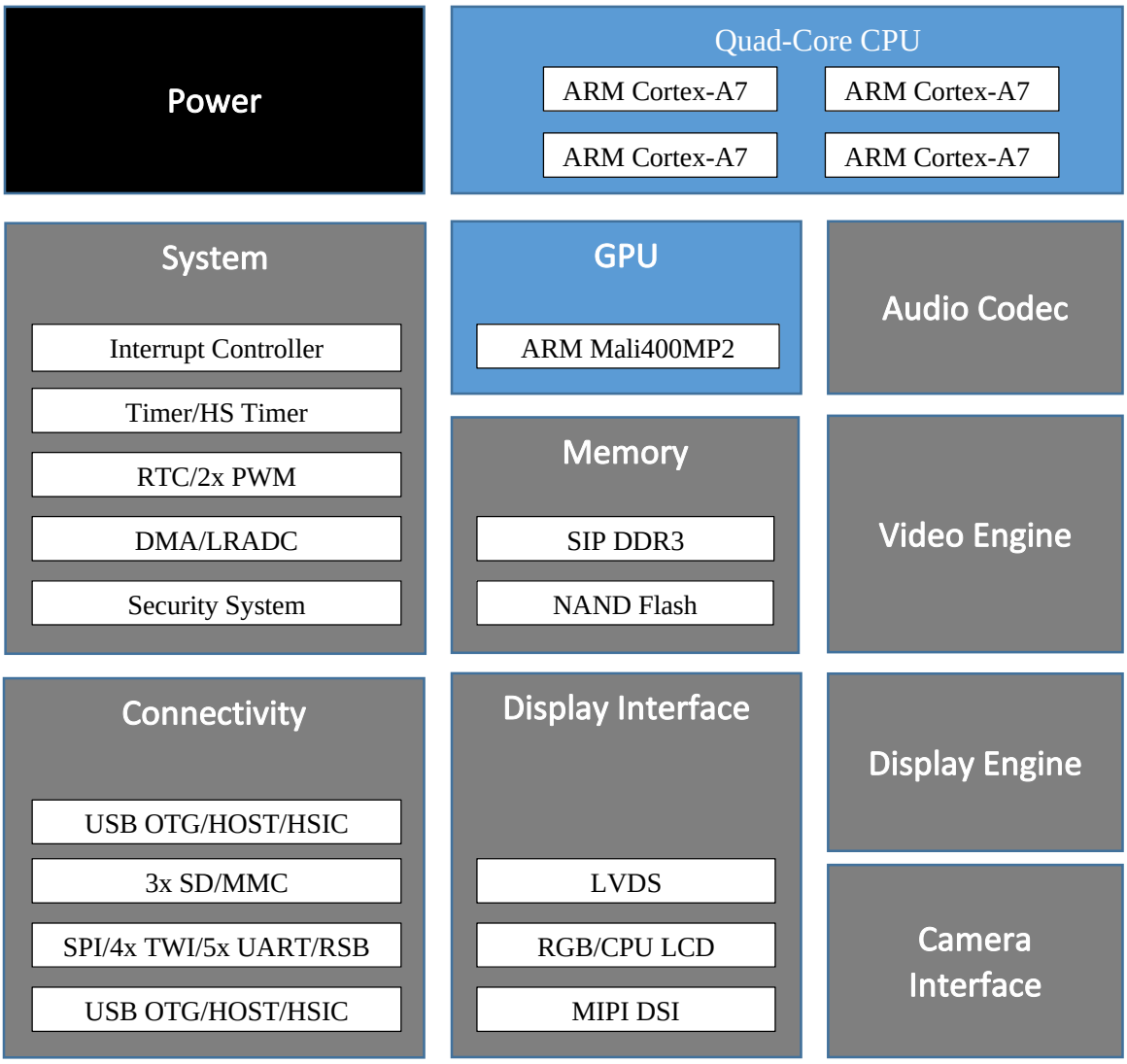


Figure 3-1. X3 Block Diagram

4. Pin Description

4.1. Pin Characteristics

Table 4-1 lists the characteristics of H500 Pins from seven aspects:BALL#,Pin Name,Default Function,Type,ResetState, Default Pull Up/Down,and Buffer Strength.

NOTES

1)Default Function defines the default function of each pin,especially for pins with multiplexing functions;

2)Type defines the signal direction:I(Input),O(Output),I/O(Input/Output),OD(Open Drain),A(Analog),AI(Analog Input), AO(Analog Output),AIO(Analog Input/Output),P(Power),G(Ground);

3)Reset State defines the state of the terminal at reset:Z for high-impedance;

4)Default Pull Up/Down defines the presence of an internal pull up or pull down resister.Unless otherwise specified, the pin is default to be floating,and can be configured as pull up or pull down;

5)Buffer Strength defines drive strength of the associated output buffer.It is tested in the condition that VCC=3.3V, strength=MAX;

Table 4-1. Pin Characteristics

Ball#	Pin Name	Default Function	Type	Reset State	Default Pull Up/Down	Buffer Strength (mA)
DRAM						
T2	DVREF	DRAM	P	Z	-	-
U2	DDRZQ	DRAM	A	Z	-	-
U1	DZQ	DRAM	A	Z	-	-
P11,P12,P13,R10,R11,R12,R13,R14	VCC-DRAM	POWER	P	-	-	-
T1	VDD-DLL	POWER	P	-	-	-
GPIO B						
B25	PB0	GPIO	I/O	Z	NO PULL	20
B24	PB1	GPIO	I/O	Z	NO PULL	20
A24	PB2	GPIO	I/O	Z	NO PULL	20
B23	PB3	GPIO	I/O	Z	NO PULL	20
A23	PB4	GPIO	I/O	Z	NO PULL	20
B22	PB5	GPIO	I/O	Z	NO PULL	20
A22	PB6	GPIO	I/O	Z	NO PULL	20
B21	PB7	GPIO	I/O	Z	NO PULL	20
GPIO C						
A9	PC0	GPIO	I/O	Z	NO PULL	20
B8	PC1	GPIO	I/O	Z	NO PULL	20
A8	PC2	GPIO	I/O	Z	NO PULL	20
B7	PC3	GPIO	I/O	Z	Pull-up	20
A7	PC4	GPIO	I/O	Z	Pull-up	20
B6	PC5	GPIO	I/O	Z	NO PULL	20
A6	PC6	GPIO	I/O	Z	Pull-up	20
B5	PC7	GPIO	I/O	Z	Pull-up	20
A5	PC8	GPIO	I/O	Z	NO PULL	20
B4	PC9	GPIO	I/O	Z	NO PULL	20

Ball#	Pin Name	Default Function	Type	Reset State	Default Pull Up/Down	Buffer Strength (mA)
A4	PC10	GPIO	I/O	Z	NO PULL	20
B3	PC11	GPIO	I/O	Z	NO PULL	20
A3	PC12	GPIO	I/O	Z	NO PULL	20
B2	PC13	GPIO	I/O	Z	NO PULL	20
A2	PC14	GPIO	I/O	Z	NO PULL	20
C1	PC15	GPIO	I/O	Z	NO PULL	20
C2	PC16	GPIO	I/O	Z	NO PULL	20
GPIO D						
X18	PD2	GPIO	I/O	Z	NO PULL	20
Y18	PD3	GPIO	I/O	Z	NO PULL	20
X17	PD4	GPIO	I/O	Z	NO PULL	20
Y17	PD5	GPIO	I/O	Z	NO PULL	20
X16	PD6	GPIO	I/O	Z	NO PULL	20
Y16	PD7	GPIO	I/O	Z	NO PULL	20
X15	PD10	GPIO	I/O	Z	NO PULL	20
Y15	PD11	GPIO	I/O	Z	NO PULL	20
X14	PD12	GPIO	I/O	Z	NO PULL	20
Y14	PD13	GPIO	I/O	Z	NO PULL	20
X13	PD14	GPIO	I/O	Z	NO PULL	20
Y13	PD15	GPIO	I/O	Z	NO PULL	20
X11	PD18	GPIO	I/O	Z	NO PULL	20
Y11	PD19	GPIO	I/O	Z	NO PULL	20
X10	PD20	GPIO	I/O	Z	NO PULL	20
Y10	PD21	GPIO	I/O	Z	NO PULL	20
X9	PD22	GPIO	I/O	Z	NO PULL	20
Y9	PD23	GPIO	I/O	Z	NO PULL	20
X8	PD24	GPIO	I/O	Z	NO PULL	20
Y8	PD25	GPIO	I/O	Z	NO PULL	20
X7	PD26	GPIO	I/O	Z	NO PULL	20
Y7	PD27	GPIO	I/O	Z	NO PULL	20
X12,Y12	VCC-PD	POWER	P	-	-	
GPIO E						
G1	PE0	GPIO	I/O	Z	NO PULL	20
G2	PE1	GPIO	I/O	Z	NO PULL	20
H1	PE2	GPIO	I/O	Z	NO PULL	20
H2	PE3	GPIO	I/O	Z	NO PULL	20
J1	PE4	GPIO	I/O	Z	NO PULL	20
J2	PE5	GPIO	I/O	Z	NO PULL	20
K1	PE6	GPIO	I/O	Z	NO PULL	20
K2	PE7	GPIO	I/O	Z	NO PULL	20
L1	PE8	GPIO	I/O	Z	NO PULL	20
L2	PE9	GPIO	I/O	Z	NO PULL	20
M1	PE10	GPIO	I/O	Z	NO PULL	20

Ball#	Pin Name	Default Function	Type	Reset State	Default Pull Up/Down	Buffer Strength (mA)
M2	PE11	GPIO	I/O	Z	NO PULL	20
N1	PE12	GPIO	I/O	Z	NO PULL	20
N2	PE13	GPIO	I/O	Z	NO PULL	20
P1	PE14	GPIO	I/O	Z	NO PULL	20
P2	PE15	GPIO	I/O	Z	NO PULL	20
R1	PE16	GPIO	I/O	Z	NO PULL	20
R2	PE17	GPIO	I/O	Z	NO PULL	20
GPIO F						
D1	PF0	GPIO	I/O	Z	NO PULL	20
D2	PF1	GPIO	I/O	Z	NO PULL	20
E1	PF2	GPIO	I/O	Z	NO PULL	20
E2	PF3	GPIO	I/O	Z	NO PULL	20
F1	PF4	GPIO	I/O	Z	NO PULL	20
F2	PF5	GPIO	I/O	Z	NO PULL	20
GPIO G						
A12	PG0	GPIO	I/O	Z	NO PULL	20
B11	PG1	GPIO	I/O	Z	NO PULL	20
A11	PG2	GPIO	I/O	Z	NO PULL	20
B10	PG3	GPIO	I/O	Z	NO PULL	20
A10	PG4	GPIO	I/O	Z	NO PULL	20
B9	PG5	GPIO	I/O	Z	NO PULL	20
A14	PG6	GPIO	I/O	Z	NO PULL	20
B13	PG7	GPIO	I/O	Z	NO PULL	20
A13	PG8	GPIO	I/O	Z	NO PULL	20
B12	PG9	GPIO	I/O	Z	NO PULL	20
A16	PG10	GPIO	I/O	Z	NO PULL	20
B15	PG11	GPIO	I/O	Z	NO PULL	20
A15	PG12	GPIO	I/O	Z	NO PULL	20
B14	PG13	GPIO	I/O	Z	NO PULL	20
GPIO H						
A19	PH0	GPIO	I/O	Z	NO PULL	20
B18	PH1	GPIO	I/O	Z	NO PULL	20
A18	PH2	GPIO	I/O	Z	NO PULL	20
B17	PH3	GPIO	I/O	Z	NO PULL	20
A17	PH4	GPIO	I/O	Z	NO PULL	20
B16	PH5	GPIO	I/O	Z	NO PULL	20
A21	PH6	GPIO	I/O	Z	NO PULL	20
B20	PH7	GPIO	I/O	Z	NO PULL	20
A20	PH8	GPIO	I/O	Z	NO PULL	20
B19	PH9	GPIO	I/O	Z	NO PULL	20
GPIO L						
P26	PL0	GPIO	I/O	Z	Pull-up	20

Ball#	Pin Name	Default Function	Type	Reset State	Default Pull Up/Down	Buffer Strength (mA)
R25	PL1	GPIO	I/O	Z	Pull-up	20
R26	PL2	GPIO	I/O	Z	NO PULL	20
T25	PL3	GPIO	I/O	Z	NO PULL	20
T26	PL4	GPIO	I/O	Z	NO PULL	20
W25	PL5	GPIO	I/O	Z	NO PULL	20
X25	PL6	GPIO	I/O	Z	NO PULL	20
Y25	PL7	GPIO	I/O	Z	NO PULL	20
X24	PL8	GPIO	I/O	Z	NO PULL	20
Y24	PL9	GPIO	I/O	Z	NO PULL	20
X23	PL10	GPIO	I/O	Z	NO PULL	20
Y23	PL11	GPIO	I/O	Z	NO PULL	20
System Control						
P25	NMI	-	I	Z	-	
K25	RESET	-	I	Z	-	
B26	Uboot	-	I	Z	Pull-up	
Audio Codec						
L26	MIC1N		A	-	-	
L25	MIC1P		A	-	-	
M26	MIC2N		A	-	-	
M25	MIC2P		A	-	-	
F26	LINEINR		A	-	-	
F25	LINEINL		A	-	-	
H26	VRA1		A	-	-	
H25	VRA2		A	-	-	
J25	VRP		A	-	-	
K26	AVCC		P	-	-	
G25	HBIAS		A	-	-	
G26	MBIAS		A	-	-	
J26	AGND		G	-	-	
E26	HPOUTR		A	-	-	
E25	HPOUTL		A	-	-	
D25	HPCOM		A	-	-	
C26	HPCOMFB		A	-	-	
C25	HPVCCBP		P	-	-	
D26	HPVCCIN		P	-	-	
USB						
Y20	USB-DM0		A	-	-	
X20	USB-DP0		A	-	-	
Y21	USB-DM1		A	-	-	
X21	USB-DP1		A	-	-	
X22	VCC-USB		P	-	-	
HSIC						
X19	HSIC-DAT		A	-	-	

Ball#	Pin Name	Default Function	Type	Reset State	Default Pull Up/Down	Buffer Strength (mA)
Y19	HSIC-STR		A	-	-	
Y22	VCC-HSIC		P	-	-	
ADC						
N26	LRADC0		A	-	-	
N25	LRADC1		A	-	-	
DSI						
X4	DSI-CKN		A	-	-	
Y4	DSI-CKP		A	-	-	
X6	DSI-D0N		A	-	-	
X5	DSI-D1N		A	-	-	
X3	DSI-D2N		A	-	-	
X2	DSI-D3N		A	-	-	
Y6	DSI-D0P		A	-	-	
Y5	DSI-D1P		A	-	-	
Y3	DSI-D2P		A	-	-	
Y2	DSI-D3P		A	-	-	
X1,Y1	VCC-DSI		P	-	-	
CLOCK						
V26	X32KIN		A	-	-	
W26	X32KOUT		A	-	-	
U26	X32KFOUT		A	-	-	
U25	RTCVIO		A	-	-	
V25	VCC-RTC		P	-	-	
V2	X24MIN		A	-	-	
V1	X24MOUT		A	-	-	
W1	VCC-PLL		P	-	-	
Power						
W2	VCC-EFUSE		P	-	-	
G16,G17,G18,H16,H17,H18,J16,J17,J18	VDD-CPUS		P	-	-	
G10,G11,G12,G13,G14,H11,H12,H13	VDD-CPU		P	-	-	
G16,G17,G18,H16,H17,H18,J16,J17,J18	VDD-SYS		P	-	-	
N17,N18,P17,P18,X23,Y26	VCC-IO		P	-	-	

N12,J12,A26,R16,R15,R9, A25,P16,P15,P14,P10,P9, B1,A1,N16,N15,N14,N13 ,N12,N11,N10,N9,M18, M17,M16,M15,M14,M1 3,M12,M11,M10,M9,L18 ,L17,L16,L15,L14,L13,L12 ,L11,L10,L9,K18,K17	GND		G	-	-	

Ball#	Pin Name	Default Function	Type	Reset State	Default Pull Up/Down	Buffer Strength(mA)
K16,K15,K14,K13,K12,K11,K10,K9,J15,J14,J13,J12,J11,J10,J9,H15,H14,H10,H9,G15,G9	GND		G	-	-	

4.2. GPIO Multiplexing Functions

The following table provides a description of the H500 GPIO multiplexing functions.

Table 4-2. Multiplexing Functions

Pin Name	Default Function	IO Type	Default IO State	Default Pull-up/down	Function 2	Function3	Function 4
PB0	GPIO	I/O	DIS	Z	UART2-TX	UART0-TX	PB-EINT0
PB1		I/O	DIS	Z	UART2-RX	UART0-RX	PB-EINT1
PB2		I/O	DIS	Z	UART2-RTS	-	PB-EINT2
PB3		I/O	DIS	Z	UART2-CTS	-	PB-EINT3
PB4		I/O	DIS	Z	PCM0-SYNC	AIF2-SYNC	PB-EINT4
PB5		I/O	DIS	Z	PCM0-BCLK	AIF2-BCLK	PB-EINT5
PB6		I/O	DIS	Z	PCM0-DOUT	AIF2-DOUT	PB-EINT6
PB7		I/O	DIS	Z	PCM0-DIN	AIF2-DIN	PB-EINT7
PC0	GPIO	I/O	DIS	Z	NAND-WE	SPI0-MOSI	-
PC1		I/O	DIS	Z	NAND-ALE	SPI0-MISO	-
PC2		I/O	DIS	Z	NAND-CLE	SPI0-CLK	-
PC3		I/O	DIS	Pull-up	NAND-CE1	SPI0-CS	-
PC4		I/O	DIS	Pull-up	NAND-CE0	-	-
PC5		I/O	DIS	Z	NAND-RE	SDC2-CLK	-
PC6		I/O	DIS	Pull-up	NAND-RB0	SDC2-CMD	-
PC7		I/O	DIS	Pull-up	NAND-RB1	-	-
PC8		I/O	DIS	Z	NAND-DQ0	SDC2-D0	-
PC9		I/O	DIS	Z	NAND-DQ1	SDC2-D1	-
PC10		I/O	DIS	Z	NAND-DQ2	SDC2-D2	-
PC11		I/O	DIS	Z	NAND-DQ3	SDC2-D3	-
PC12		I/O	DIS	Z	NAND-DQ4	SDC2-D4	-
PC13		I/O	DIS	Z	NAND-DQ5	SDC2-D5	-
PC14		I/O	DIS	Z	NAND-DQ6	SDC2-D6	-
PC15		I/O	DIS	Z	NAND-DQ7	SDC2-D7	-
PC16		I/O	DIS	Z	NAND-DQS	SDC2-RST	-
PD2	GPIO	I/O	DIS	Z	LCD-D2	SDC1-CLK	-
PD3		I/O	DIS	Z	LCD-D3	SDC1-CMD	-
PD4		I/O	DIS	Z	LCD-D4	SDC1-D0	-
PD5		I/O	DIS	Z	LCD-D5	SDC1-D1	-
PD6		I/O	DIS	Z	LCD_D6	SDC1-D2	-

Pin Name	Default Function	IO Type	Default IO State	Default Pull-up/down	Function 2	Function3	Function 4
PD7		I/O	DIS	Z	LCD-D7	SDC1-D3	-
PD10		I/O	DIS	Z	LCD-D10	UART1-TX	-
PD11		I/O	DIS	Z	LCD-D11	UART1-RX	-
PD12		I/O	DIS	Z	LCD-D12	UART1-RTS	-
PD13		I/O	DIS	Z	LCD-D13	UART1-CTS	-
PD14		I/O	DIS	Z	LCD-D14	-	-
PD15		I/O	DIS	Z	LCD-D15	-	-
PD18		I/O	DIS	Z	LCD-D18	LVDS-VP0	-
PD19		I/O	DIS	Z	LCD-D19	LVDS-VN0	-
PD20		I/O	DIS	Z	LCD-D20	LVDS-VP1	-
PD21		I/O	DIS	Z	LCD-D21	LVDS-VN1	-
PD22		I/O	DIS	Z	LCD-D22	LVDS-VP2	-
PD23		I/O	DIS	Z	LCD-D23	LVDS-VN2	-
PD24		I/O	DIS	Z	LCD-CLK	LVDS-VPC	-
PD25		I/O	DIS	Z	LCD-DE	LVDS-VNC	-
PD26		I/O	DIS	Z	LCD-HSYNC	LVDS-VP3	-
PD27		I/O	DIS	Z	LCD-VSYNC	LVDS-VN3	-
PE0	GPIO	I/O	DIS	Z	CSI-PCLK	-	-
PE1		I/O	DIS	Z	CSI-MCLK	-	-
PE2		I/O	DIS	Z	CSI-HSYNC	-	-
PE3		I/O	DIS	Z	CSI-VSYNC	-	-
PE4		I/O	DIS	Z	CSI-D0	-	-
PE5		I/O	DIS	Z	CSI-D1	-	-
PE6		I/O	DIS	Z	CSI-D2	-	-
PE7		I/O	DIS	Z	CSI-D3	-	-
PE8		I/O	DIS	Z	CSI-D4	-	-
PE9		I/O	DIS	Z	CSI-D5	-	-
PE10		I/O	DIS	Z	CSI-D6	-	-
PE11		I/O	DIS	Z	CSI-D7	-	-
PE12		I/O	DIS	Z	CSI-SCK	TWI2-SCK	-
PE13		I/O	DIS	Z	CSI-SDA	TWI2-SDA	-
PE14		I/O	DIS	Z	-	-	-
PE15		I/O	DIS	Z	-	-	-
PE16		I/O	DIS	Z	-	-	-
PE17		I/O	DIS	Z	-	-	-
PF0	GPIO	I/O	JTAG	Z	SDC0-D1	JTAG-MS1	-
PF1		I/O	JTAG	Z	SDC0-D0	JTAG-DI1	-
PF2		I/O	DIS	Z	SDC0-CLK	UART0-TX	-
PF3		I/O	JTAG	Z	SDC0-CMD	JTAG-DO1	-
PF4		I/O	DIS	Z	SDC0-D3	UART0-RX	-
PF5		I/O	JTAG	Z	SDC0-D2	JTAG-CK1	-
PG0	GPIO	I/O	DIS	Z	SDC1-CLK	-	PG-EINT0
PG1		I/O	DIS	Z	SDC1-CMD	-	PG-EINT1

Pin Name	Default Function	IO Type	Default IO State	Default Pull-up/down	Function 2	Function3	Function 4
PG2		I/O	DIS	Z	SDC1-D0	-	PG-EINT2
PG3		I/O	DIS	Z	SDC1-D1	-	PG-EINT3
PG4		I/O	DIS	Z	SDC1-D2	-	PG-EINT4
PG5		I/O	DIS	Z	SDC1-D3	-	PG-EINT5
PG6		I/O	DIS	Z	UART1-TX	-	PG-EINT6
PG7		I/O	DIS	Z	UART1-RX	-	PG-EINT7
PG8		I/O	DIS	Z	UART1-RTS	-	PG-EINT8
PG9		I/O	DIS	Z	UART1-CTS	-	PG-EINT9
PG10		I/O	DIS	Z	PCM1-SYNC	AIF3-SYNC	PG-EINT10
PG11		I/O	DIS	Z	PCM1-BCLK	AIF3-BCLK	PG-EINT11
PG12		I/O	DIS	Z	PCM1-DOUT	AIF3-DOUT	PG-EINT12
PG13		I/O	DIS	Z	PCM1-DIN	AIF3-DIN	PG-EINT13
PH0	GPIO	I/O	DIS	Z	PWM0	-	-
PH1		I/O	DIS	Z	PWM1	-	-
PH2		I/O	DIS	Z	TWI0-SCK	-	-
PH3		I/O	DIS	Z	TWI0-SDA	-	-
PH4		I/O	DIS	Z	TWI1-SCK	-	-
PH5		I/O	DIS	Z	TWI1-SDA	-	-
PH6		I/O	DIS	Z	SPI0-CS	UART3-TX	-
PH7		I/O	DIS	Z	SPI0-CLK	UART3-RX	-
PH8		I/O	DIS	Z	SPI0-MOSI	UART3-RTS	-
PH9		I/O	DIS	Z	SPI0-MISO	UART3-CTS	-
PL0	GPIO	I/O	DIS	Pull-up	S-RSB-SCK	S-TWI-SCK	S-PL-EINT0
PL1		I/O	DIS	Pull-up	S-RSB-SDA	S-TWI-SDA	S-PL-EINT1
PL2		I/O	DIS	Z	S-UART-TX	-	S-PL-EINT2
PL3		I/O	DIS	Z	S-UART-RX	-	S-PL-EINT3
PL4		I/O	DIS	Z	S-JTAG-MS	-	S-PL-EINT4
PL5		I/O	DIS	Z	S-JTAG-CK	-	S-PL-EINT5
PL6		I/O	DIS	Z	S-JTAG-DO	-	S-PL-EINT6
PL7		I/O	DIS	Z	S-JTAG-DI	-	S-PL-EINT7
PL8		I/O	DIS	Z	S-TWI-SCK	-	S-PL-EINT8
PL9		I/O	DIS	Z	S-TWI-SDA	-	S-PL-EINT9
PL10		I/O	DIS	Z	S-PWM	-	S-PL-EINT10
PL11		I/O	DIS	Z	-	-	S-PL-EINT11

4.3. Detailed Pin/Signal Description

Table 4-3 shows the detailed function of every pin/signal based on the different interface.

Table 4-3.Detailed Pin Description

Pin/Signal Name	Description	Type
DRAM		

Pin/Signal Name	Description	Type

DDRZQ	SIP DDR3 ZQ Calibration	A
DZQ	DRAM Controller ZQ Calibration	A
DVREF	DRAM Reference Input	P
VCC-DRAM	DRAM Power Supply	P
VDD-DLL	DLL Power Supply	P
System Control		
NMI	Non-Maskable Interrupt	I
RESET	Reset Signal	I
uboot	Boot mode select	I
USB		
USB-DM0	USB2.0 Differential Data Signal	AIO
USB-DP0		AIO
USB-DM1	USB2.0 Differential Data Signal	AIO
USB-DP1		AIO
VCC-USB	USB2.0 Analog Voltage	P
HSIC		
VCC12-HSIC	HSIC Voltage	P
HSIC-STR	USB HSIC Strobe Signal	AIO
HSIC-DAT	USB HSIC Data Signal	AIO
ADC		
LRADC0/1	Key Input	AI
Audio Codec		
MICINN[2:1]	Microphone Differential Input Signal	AI
MICINP[2:1]		AI
LINEINR	Line-in Right Input	AI
LINEINL	Line-in Left Input	AI
HBIAS	Analog Headphone Bias	AO
MBIAS	Analog Microphone Bias	AO

Pin/Signal Name	Description	Type
VRA1	Reference Voltage	AO
VRA2	Reference Voltage	AO
VRP	Reference Voltage	AO
AVCC	Analog Voltage	P
AGND	Analog GND	G
HPOUTR	Headphone Right Channel Output	AO
HPOUTL	Headphone Light Channel Output	AO
HPVCCIN	Headphone Voltage Supply	P
HPVCCBP	Headphone Voltage Bypass	AO
HPCOM	HPCOM Output	AO
HPCOMFB	HPCOM Feedback Input	AI
HPBP	HPVCC Bypass Output	AO
DSI		
DSI-DP0	MIPI DSI Differential Signal	AIO
DSI-DN0		AIO
DSI-DP1	MIPI DSI Differential Signal	AO

DSI-DN1		AO
DSI-DP2	MIPI DSI Differential Signal	AO
DSI-DN2		AO
DSI-DP3	MIPI DSI Differential Signal	AO
DSI-DN3		AO
DSI-CKP	MIPI DSI Differential Clock	AO
DSI-CKN		AO
VCC-DSI	MIPI DSI Voltage	P
CLOCK		
X32KIN	Clock Input Of 32KHz Crystal	AI
X32KOUT	Clock Output Of 32KHz Crystal	AO
X32KFOUT	32KHz Feedback Output	OD
VCC-RTC	RTC Voltage	P
RTC-VIO	Internal LDO Output	P
X24MIN	Clock Input Of 24MHz Crystal	AI
X24MOUT	Clock Output Of 24MHz Crystal	AO
VCC-PLL	PLL Analog Voltage	P
SD /MMC(x=[2:0])		
SDCx-CMD	SDx/MMCx/SDIOx Command Signal	I/O
SDCx-CLK	SDx/MMCx/SDIOx Clock Signal	O
SDC0-D[3:0]	SD0/MMC0/SDIO0 Data Signal	I/O
SDC1-D[3:0]	SD1/MMC1/SDIO1 Data Signal	I/O
SDC2-D[7:0]	SD2/MMC2/SDIO2 Data Signal	I/O
SDC2-RST	SD2/MMC2/SDIO2 Reset Signal	O
NAND FLASH		
NAND-DQ[7:0]	NAND Flash Data Signal	I/O
NAND-DQS	NADN Flash Data Strobe Signal	I/O
NAND-WE	NAND Flash Write Enable	O

Pin/Signal Name	Description	Type
NAND-RE	NAND Flash Read Enable	O
NAND-ALE	NAND Flash Address Latch Enable	O
NAND-CLE	NAND Flash Command Latch Enable	O
NAND-CE[1:0]	NAND Flash Chip Select [1:0]	O
NAND-RB[1:0]	NAND Flash Ready/Busy Bit	I
RSB		
S-RSB-SCK	RSB Clock Signal	O
S-RSB-SDA	RSB Data Signal	I/O
Interrupt		
PB-EINT[10:0]	GPIO B Interrupt	I
PG-EINT[13:0]	GPIO G Interrupt	I
S-PL-EINT[12:0]	GPIO L Interrupt	I
PWM		
S_PWM	Pulse Width Modulation output	O
PWM	Pulse Width Modulation output	O

LCD		
LCD0-D[23:0]	LCD Data Signal	O
LCD-CLK	LCD Clock Output	O
LCD-DE	LCD Data Enable	O
LCD-HSYNC	LCD Horizontal SYNC	O
LCD-VSYNC	LCD Vertical SYNC	O
LVDS		
LVDS-VP[3:0]	LVDS Differential Data Signal Output	AO
LVDS-VN[3:0]		AO
LVDS-VPC	LVDS Differential Clock Output	AO
LVDS-VNC		AO
PCM (x=[1:0])		
PCM0-SYNC	I2S/PCM SYNC	I/O
PCMx-CLK	I2S/PCM Clock	I/O
PCMx-DIN	I2S/PCM Data Input	I
PCMx-DOUT	I2S/PCM Data Output	O
CSI		
CSI-PCLK	CSI Pixel Clock	I
CSI-MCLK	CSI Master Clock	O
CSI-HSYNC	CSI Horizontal SYNC	I
CSI-VSYNC	CSI Vertical SYNC	I
CSI-D[7:0]	CSI Data Signal	I
CSI-SCK	CSI Control Clock Signal	I/O
CSI-SDA	CSI Control Data Signal	I/O
SPI		
SPI0-CS	SPI Chip Select Signal	I/O
SPI0-CLK	SPI Clock	I/O
SPI0-MOSI	SPI Mater Output ,Slave Input	I/O
SPI0-MISO	SPI Master Input ,Slave Output	I/O

Pin/Signal Name	Description	Type
UART (x=[3:0])		
UARTx-CTS	UART Data Clear to Send	I
UARTx-RTS	UART Data Request to Send	O
UARTx-TX	UART Data Transmit	O
UARTx-RX	UART Data Receive	I
S-UART-TX	UART Data Transmit	O
S-UART-RX	UART Data Receive	I
TWI (x=[2:0])		
TWIx-SCK	TWI Clock Signal	I/O
TWIx-SDA	TWI Data Signal	I/O
S-TWI-SCK	TWI Clock Signal	I/O
S-TWI-SDA	TWI Data Signal	I/O

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

Functional operation of the device at these or any other conditions beyond the absolute maximum ratings listed in Table 5-1 can cause permanent damage to the device.

Table 5-1.Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
T_{STG}	Storage Temperature	-40	125	°C
$I_{I/O}$	In/Out Current for Input and Output	-40	40	mA
VCC-IO	Power Supply for I/O	-0.3	3.6	V
VDD-DLL	Power Supply for DLL	-0.3	2.75	V
VCC-DRAM	Power Supply for DDR3/DDR3L	-0.3	1.65	V
VCC-PLL	Power Supply for PLL	-0.3	3.6	V
VCC-RTC	Power Supply for RTC	-0.3	3.6	V
AVCC	Power Supply for Analog Part	-0.3	3.6	V
VCC-USB	Power Supply for USB	-0.3	3.6	V
VCC-DSI	Power Supply for MIPI-DSI	-0.3	3.6	V
VDD-CPU	Power Supply for CPU	-0.3	1.5	V
VDD-SYS	Power Supply for System	-0.3	1.5	V

5.2. Recommended Operating Conditions

All H500 modules are used under the operating Conditions contained in Table 5-2.

Table 5-2.Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Ambient Operating Temperature	-20	-	+70	°C
VCC-IO	Power Supply for I/O	2.7	3.0	3.45	V
VDD-DLL	Power Supply for DLL	2.35	2.5	2.65	V
VCC-DRAM	Power Supply for DDR3L	1.425	1.5	1.575	V
	Power Supply for DDR3	1.425	1.5	1.575	V
VCC-PLL	Power Supply for PLL	2.9	3.0	3.6	V
VCC-USB	Power Supply for USB	2.9	3.0	3.45	V
VCC-RTC	Power Supply for RTC	2.7	3.0	3.3	V
AVCC	Power Supply for Analog Part	2.91	3.0	3.09	V
VCC-DSI	Power Supply for MIPI-DSI	2.9	3.0	3.6	V
VDD-CPU	Power Supply for CPU	1.0	-	1.32	V
VDD-SYS	Power Supply for System	0.99	1.1	1.21	V

5.3. DC Electrical Characteristics

Table 5-3 summarizes the DC electrical characteristics of H500.

Table 5-3. DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage	0.7*VCC-IO	-	VCC-IO + 0.3	V
V_{IL}	Low-Level Input Voltage	-0.3	-	0.3*VCC-IO	V
R_{PU}	Input Pull-up Resistance	50	100	150	KΩ
R_{PD}	Input Pull-down Resistance	50	100	150	KΩ
V_{HYS}	Hysteresis Voltage	0.1 x VCC-IO	-	-	V
I_{IH}	High-Level Input Current	-	-	10	uA
I_{IL}	Low-Level Input Current	-	-	10	uA
V_{OH}	High-Level Output Voltage	VCC-IO -0.2	-	VCC-IO	V
V_{OL}	Low-Level Output Voltage	0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current	-10	-	10	uA
C_{IN}	Input Capacitance	-	-	5	pF
C_{OUT}	Output Capacitance	-	-	5	pF

5.4. Oscillator Electrical Characteristics

The H500 contains two oscillators:a 24MHz oscillator and a 32768Hz oscillator.Each oscillator requires a specific crystal.The H500 device operation requires the following two input clocks:
The 32768Hz frequency is used for low frequency operation.
The 24.000MHz frequency is used to generate the main source clock of the H500 device.

Table 5-4. 24MHz Oscillator Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
1/(t_{CPMAIN})	Crystal Oscillator Frequency Range	-	24.000	-	MHz
t_{ST}	Startup Time	–	–		ms
	Frequency Tolerance at 25 °C	-40	–	+40	ppm
	Oscillation Mode	Fundamental			–
	Maximum Change Over Temperature Range	-50	–	+50	ppm
P_{ON}	Drive Level	–	–	50	uW
C_L	Equivalent Load Capacitance	–		–	pF
CL1,CL2	Internal Load Capacitance(CL1=CL2)	–		–	pF
R_S	Series Resistance(ESR)	–		–	Ω
	Duty Cycle	30	50	70	%
C_M	Motional Capacitance	–	–		pF
C_{SHUT}	Shunt Capacitance	–	–		pF
R_{BIAS}	Internal Bias Resistor				MΩ

Table 5-5. 32768Hz Oscillator Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
1/(t_{CPMAIN})	Crystal Oscillator Frequency Range	–	32768	–	Hz
t_{ST}	Startup Time	–	–		ms
	Frequency Tolerance at 25 °C	-50	–	+50	ppm
	Oscillation Mode	Fundamental			–
	Maximum Change Over Temperature Range	-50	–	+50	ppm

P_{ON}	Drive Level	–	–	50	uW
C_L	Equivalent Load Capacitance	–	–	–	pF
CL1,CL2	Internal Load Capacitance(CL1=CL2)	–	–	–	pF
R_S	Series Resistance(ESR)	–	–	–	Ω
	Duty Cycle	30	50	70	%
C_M	Motional Capacitance	–	–	–	pF
C_{SHUT}	Shunt Capacitance	–	–	–	pF
R_{BIAS}	Internal Bias Resistor	–	–	–	MΩ

5.5. Power on and Power off Sequence

The external voltage regulator and other power-on devices must provide the processor with a specific sequence of power and resets to ensure proper operations.Following figure 5-1 and figure 5-2 illustrate the poweron and off sequence.In power on sequence,VDD-DLL,VDD-SYS,VCC-DRAM,VDD-CPUS can be ramped up simultaneously at time T1.ACC,VCC-IO,VCC-3V0,VDD-CPU can be ramped up at time T2 after VDD-DLL,VDD-SYS,VCC-DRAM,VDD-CPUS are powered on.The delay time between T1 and T2 is 16ms by default.The ramping up time of each power rail is within 2ms.At time T3,all power rails reaches stable.AP-RESET#must be held low before time T4. The delay timeΔT between time T3 and time T4 is no less than 32ms.The value ofΔT can be changed by software.

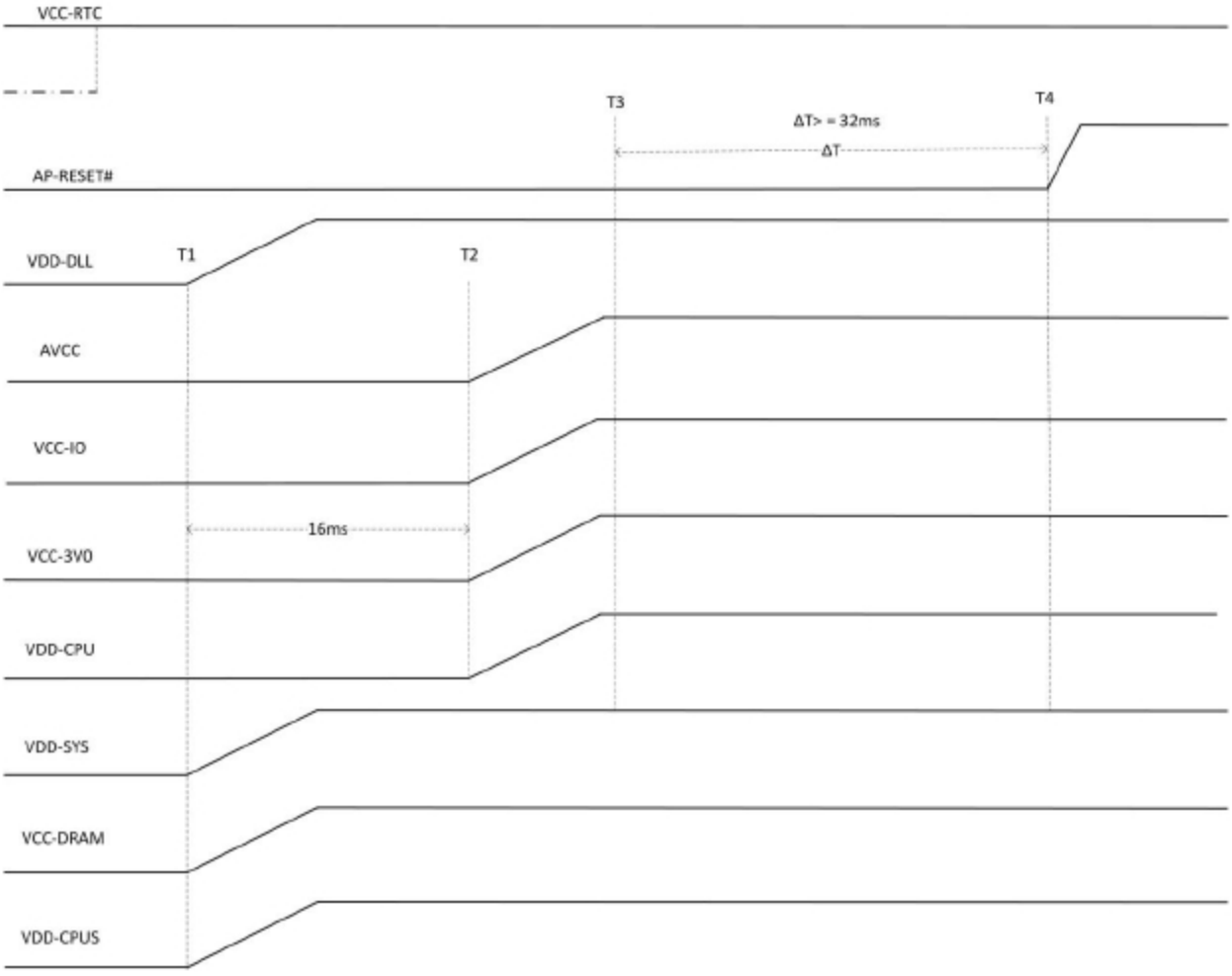


Figure 5-1.Power On Timing

The power down solution is achieved by setting AP_RESET#to 0.When AP_RESET#powered down,then all power supplies start to ramp down except VCC_RTC.The ramping down rate of each power is decided by the load on that power supply.

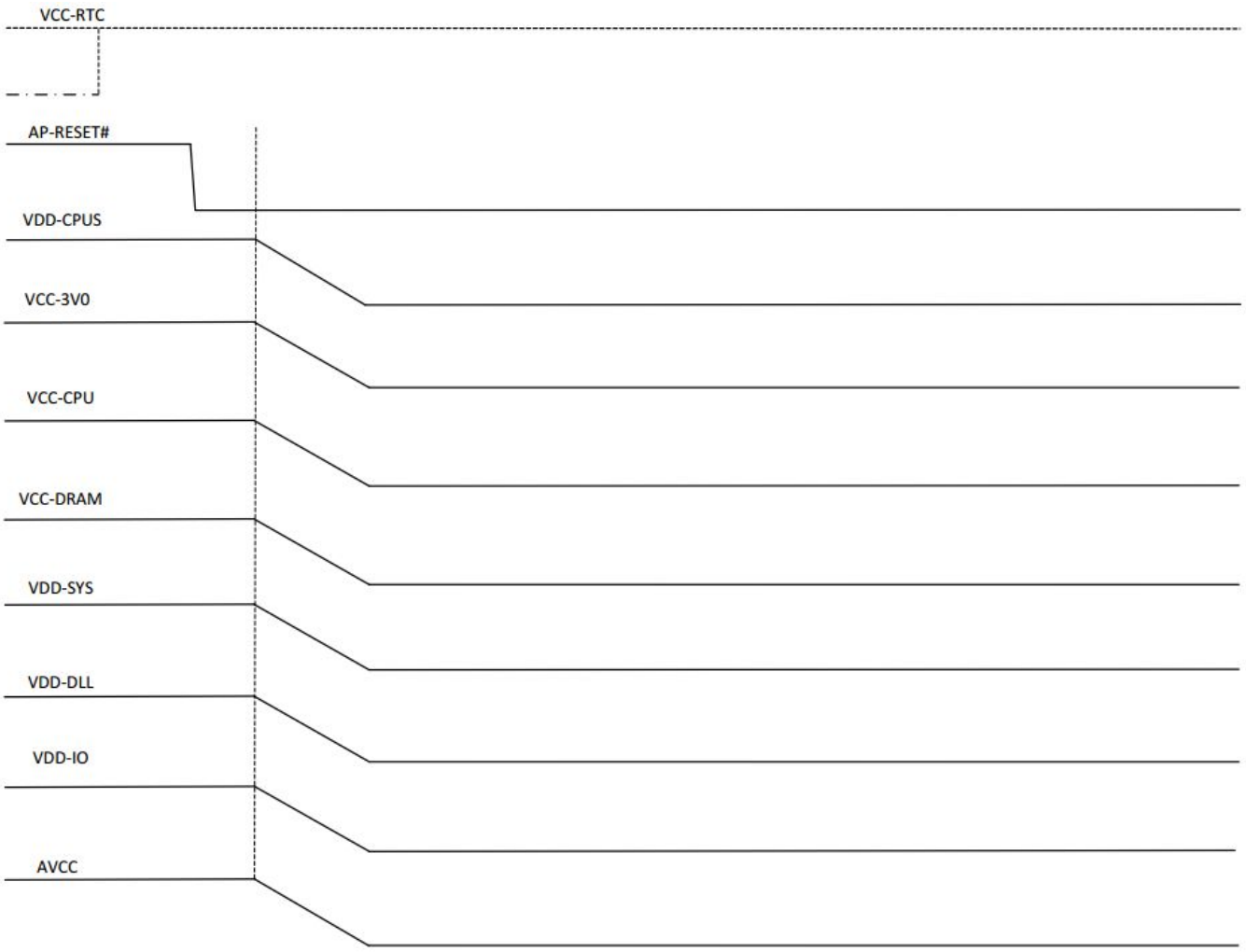


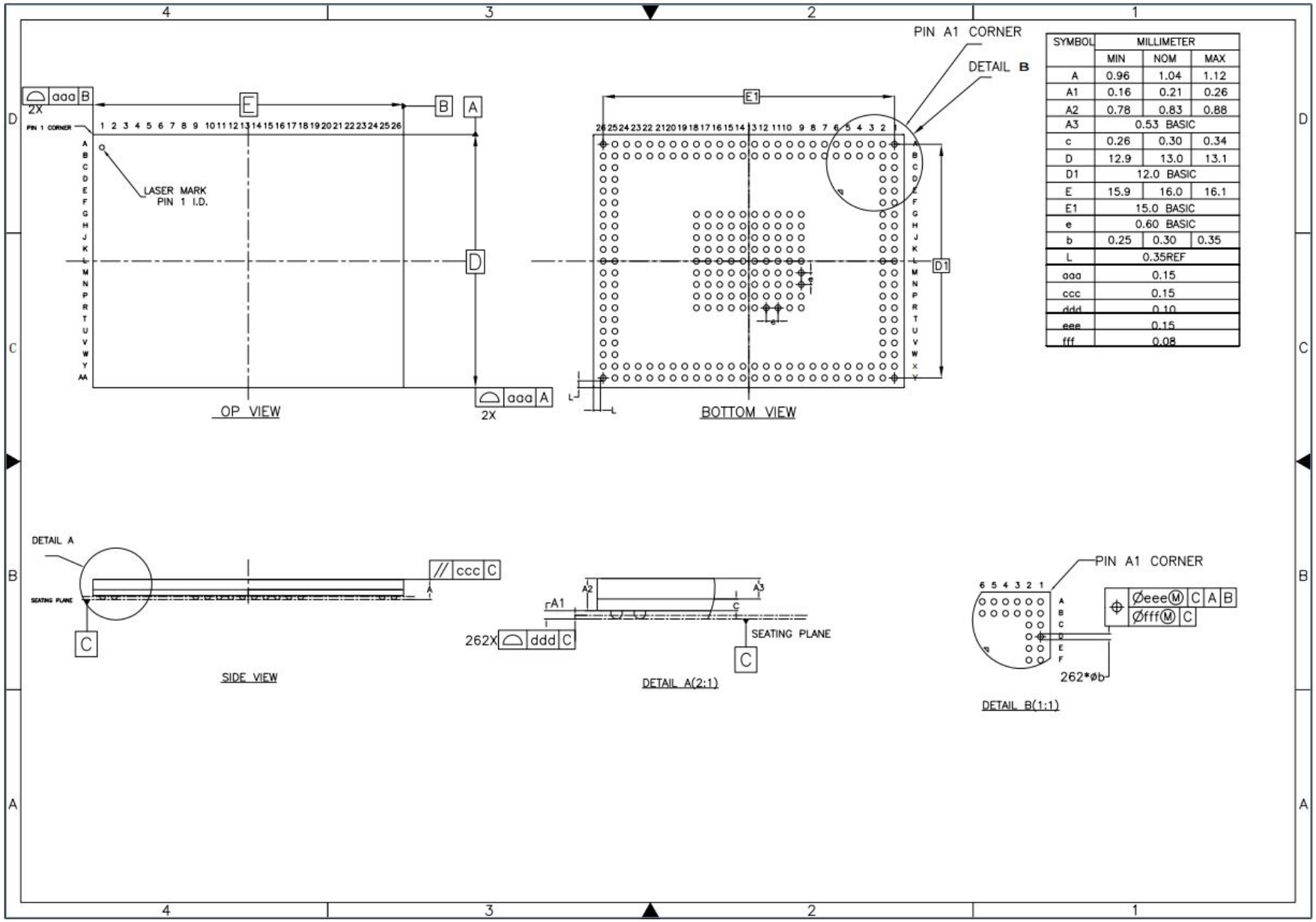
Figure 5-2. Power Down Timing

6. Pin Assignment

6.1. Pin Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	GND	PC14	PC12	PC10	PC8	PC6	PC4	PC2	PC0	PG4	PG2	PG0	PG8	PG6	PG12	PG10	PH4	PH2	PH0	PH8	PH6	PB6	PB4	PB2	GND	GND
B	GND	PC13	PC11	PC9	PC7	PC5	PC3	PC1	PG5	PG3	PG1	PG9	PG7	PG13	PG11	PH5	PH3	PH1	PH9	PH7	PB7	PB5	PB3	PB1	PB0	UBOOT
C	PC15	PC16																							HPVCCBP	HPCOMFB
D	PF0	PF1																							HPCOM	HPVCCIN
E	PF2	PF3																							HPOUTL	HPOUTR
F	PF4	PF5																							LINEINL	LINEINR
G	PE0	PE1							GND	VDD-CPU	VDD-CPU	VDD-CPU	VDD-CPU	VDD-CPU	GND	VDD-SYS	VDD-SYS	VDD-SYS							HBIAS	MBIAS
H	PE2	PE3							GND	GND	VDD-CPU	VDD-CPU	VDD-CPU	GND	GND	VDD-SYS	VDD-SYS	VDD-SYS							VRA2	VRA1
J	PE4	PE5							GND	GND	GND	GND	GND	GND	GND	VDD-SYS	VDD-SYS	VDD-SYS							VRP	AGND
K	PE6	PE7							GND	GND	GND	GND	GND	GND	GND	GND	GND	GND							RESET	AVCC
L	PE8	PE9							GND	GND	GND	GND	GND	GND	GND	GND	GND	GND							MIC1P	MIC1N
M	PE10	PE11							GND	GND	GND	GND	GND	GND	GND	GND	GND	GND							MIC2P	MIC2N
N	PE12	PE13							GND	GND	GND	GND	GND	GND	GND	GND	VCC-IO	VCC-IO							LRADC1	LRADC0
P	PE14	PE15							GND	GND	VCC-DRAM	VCC-DRAM	VCC-DRAM	GND	GND	GND	VCC-IO	VCC-IO							NMI	PL0
R	PE16	PE17							GND	VCC-DRAM	VCC-DRAM	VCC-DRAM	VCC-DRAM	VCC-DRAM	GND	GND	VDD-CPUS	VDD-CPUS							PL1	PL2
T	VDD-DLL	DVREF																							PL3	PL4
U	DZQ	DDRZQ																							RTCVIO	X32KFOUT
V	X24MOUT	X24MIN																							VCC-RTC	X32KIN
W	VCC-PLL	VCC-EFUS																							PL5	X32KOUT
X	VCC-DSI	DSI-D3N	DSI-D2N	DSI-CKN	DSI-D1N	DSI-D0N	PD26	PD24	PD22	PD20	PD18	VCC-PD	PD14	PD12	PD10	PD6	PD4	PD2	HSIC-DAT	USB-DP0	USB-DP1	VCC-USB	PL10	PL8	PL6	VCC-IO
Y	VCC-DSI	DSI-D3P	DSI-D2P	DSI-CKP	DSI-D1P	DSI-D0P	PD27	PD25	PD23	PD21	PD19	VCC-PD	PD15	PD13	PD11	PD7	PD5	PD3	HSIC-STR	USB-DM0	USB-DM1	VCC-HSIC	PL11	PL9	PL7	VCC-IO

6.2. Package Dimension



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.96	1.04	1.12
A1	0.16	0.21	0.26
A2	0.78	0.83	0.88
A3		0.53 BASIC	
c	0.26	0.30	0.34
D	12.9	13.0	13.1
D1		12.0 BASIC	
E	15.9	16.0	16.1
E1		15.0 BASIC	
e		0.60 BASIC	
b	0.25	0.30	0.35
L		0.35REF	
aaa		0.15	
ccc		0.15	
ddd		0.10	
eee		0.15	
fff		0.08	